

### **REMARKS**

Claims 1-4 and 8 have been amended. No claims have been added or canceled. Accordingly, claims 1-15 remain pending in this application.

#### **35 U.S.C. §112**

Claim 8 has been amended to overcome the rejection under this section. Specifically, claim 8 now recites that the repetition number counting unit includes a transfer number register. This amendment is supported at page 21, lines 16-23 of the specification.

#### **35 U.S.C. §§102 and 103**

Claims 1-8 and 10-15 stand rejected under 35 U.S.C. §102(b) as being anticipated by Mitsuhiro et al (U.S. Patent No. 5,325,489). Claims 9 and 15 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Mitsuhiro et al. These rejections are traversed as follows.

The present invention is a data transfer controller, and a data processor that includes the data transfer controller. The data transfer controller of the invention is initially set with the source address information and the destination address information. A control unit increments the transfer destination address in response to each data transferring. The control unit issues an interrupt each time when a

transferred data number reaches a predetermined number. The control unit initializes the transfer destination address after the interrupt has been issued for a predetermined plurality of times, and continues data transferring operations to the initialized transfer destination address. Thus, the data transfer controller resets the destination address information when outputting the interrupt signal at predetermined times.

The Mitsuhiro et al. reference discloses a data transfer controller (DMA Controller 105) that controls data transfer based upon a DMA Control Register 201. The data transfer controller controls data transferring from a DMA Transfer Area A, and continues the data transferring from the DMA transferring Area B after completing data transferring from the DMA Transferring Area A in accordance with a DMA Authorization Bit 202. The data transfer controller issue an interrupt signal upon completion of data transferring to the DMA Transfer Area A (FIGS. 4-5). However, Mitsuhiro et al. disclose two registers MAR 208 for address setting of the DMA Transfer Area A, and NMAR 209 for address setting of the DMA Transfer Area B. The data transfer controller changes the first register MAR 208 to the second register NMAR 209 upon completion of data transferring to the DMA Transfer Area A. Thus, Mitsuhiro et al. disclose that the data transfer controller issues the interrupt signal in accordance with the changing of data transfer information, for each change of memory area. (See, e.g., column 6, lines 21-55 of Mitsuhiro et al.) Whereas in the present invention, after the interrupt has been issued a predetermined number of times, the transfer destination address is initialized. Claim 3 contains similar

limitations to claim 1 with respect to initializing the transfer destination address after the interrupt has been issued a predetermined plurality of times. Thus, claims 1 and 3 are patentable over Mitsuhira et al. because the recited structure and functionality enables the use of two or more memory areas, while Mitsuhira et al. does not teach such a structure.

Furthermore, claim 2 recites that the controller changes the transfer destination address to a second transfer start address after the interrupt has been issued a predetermined number of times, and restarts the data transferring to the changed transfer destination address. Mitsuhira, on the other hand, only teaches the use of a single address, and does not teach changing the transfer destination address to a second start address after the interrupt has been issued a predetermined number of times. Thus, claim 2 also sets forth a function different from that of Mitsuhira et al. because alternate memory areas may be utilized.

Also, amended claim 4 sets forth that the control unit outputs an interrupt signal each time the transfer number counting unit counts up to a first target number, and sets the first transfer control address information to a temporary register as the second transfer control address information from the initial address register each time the repetition number counting unit counts up to a second target number. Mitsuhira does not teach a control unit that sets the first transfer control address information to a temporary register as a second transfer control address information each time a repetition number counting unit counts up to a second target number. Thus, claim 4 also sets forth a structure and functionality that is different than that

taught by Mitsuhiro et al., and which also enables use of two or more memory areas. Accordingly, claims 1-4 are patentable over Mitsuhiro and the other art of record, taken either singly, or in combination. The remaining claims depend from these claims, and are patentable at least because they depend from allowable base claims.

**Conclusion**

In view of the foregoing, Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Respectfully submitted,



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